CUSTOMIZABLE SIMULATION MODEL OF AN ATM/SONET FRAMER FOR SYSTEM LEVEL VERIFICATION AND PERFORMANCE CHARACTERIZATION

Technical Field

The technical field of this invention relates to a customizable model of an ATM/SONET Framer for system level verification and performance characterization with programmable FIFO status update and clock domain synchronization.

Background of the Invention and Prior Art

A system level simulation requires use of behavioral models representing functionality of commercial off-the-shelf MAC devices from many vendors. Such behavioral models are generally not available from the device vendors. A solution to this problem commonly suggested by the device vendors is to use the actual Register Transfer Level (RTL) or gate level design MODEL implemented in a Hardware Description Language (HDL) such as Verilog or VHDL. However, using a non-behavioral model in a simulation results in significant degradation of simulation performance. Moreover, integration of the actual design model or vendor supplied behavioral model

in the local simulation limits observability and controllability due to constraints stemming from the protection of proprietary data. A practical alternative to this problem is to develop an accurate custom behavioral model that offers sufficient parameters which can be programmed to represent framers from different vendors.

Summary of the Invention

The present invention describes the architecture and implementation of a behavioral VHDL model of an ATM/SONET framer. The model is comprised of two independently configurable components, a Receiver and a Transmitter, and offers flexibility to allow testing with multiple vendors' of framers by changing programmable parameters of the model.

The present invention represents a customizable simulation model of an ATM/SONET Framer for System Level Verification and Performance Characterization. An asynchronous Transfer Mode (ATM) data processing ASIC interfaces with a Media Access Control (MAC) device that presents an electrical data path interface, called Universal Test & Operations PHY Interface for ATM (UTOPIA), using ATM protocol on the ASIC side and simplex

optical interfaces using synchronous Optical Network (SONET) protocol on the network side. Such a MAC device, commonly referred to as ATM/SONET Framer, provides one Receive and one Transmit interface to the network at various SONET line rates such as 155.52 Mbps(OC-3), 622.08 Mbps(OC-12), 2488.32 Mbps(OC-48), etc. The ATM and the SONET interfaces operate on different clock frequencies and thus represent two distinct clocking domains. The data interchange between the two clocking domains is achieved via FIFO buffer elements and associated control and status signals.

Brief Description of the Drawings

Fig. 1 This figure represents the basic architecture of the ATM/SONET FRAMER.

Fig. 2 This represents SONET OC-Nc FRAME Structure.

Detailed Description of the Preferred Embodiment

Before going into the details of the present invention, it would be quite helpful to the reader to

have several terms of art defined. These are listed below:

Definitions

Sonet This is an acronym for Synchronous Optical Network. A category of fiber optic communication standards that permits extremely high speed transmission (51.84 Mbps to 24488 Mbps).

ATM This is referred to as an Asychronous Transfer Mode.

MAC is defined as the acronym, Media Access Control.

HDL is defined as the acronym, Hardware Description Language.

RTL is defined as the acronym,Register Transfer language.

VHDL & Verilog are considered as hardware description language.

As noted above, an Asynchronous Transfer Mode (ATM) data processing ASIC interfaces with a Media Access Control (MAC) device that presents an electrical data path interface, called Universal Test & Operations PHY Interface for ATM (UTOPIA), using ATM protocol on the

ASIC side and simplex optical interfaces using Synchronous Optical Network (SONET) protocol on the network side. Such a MAC device, commonly referred to as ATM/SONET Framer, provides one Receive and one Transmit interface to the network at various SONET line rates such as 155.52 Mbps(OC-3), 622.08 Mbps(OC-12), 2488.32 Gbps(OC-48), etc. The ATM and the SONET interfaces operate on different clock frequencies and thus represent two distinct clocking domains. The data interchange between the two clocking domains is achieved via FIFO buffer elements and associated control and status signals.

A system level simulation requires use of behavioral models representing functionality of commercial off-the-shelf MAC devices from many vendors. Such behavioral models are generally not available from the device vendors. A solution to this problem commonly suggested by the device vendors is to use the actual Register Transfer Level (RTL) or gate level design implemented in a Hardware Description Language (HDL) such as Verilog or VHDL. However, using a non-behavioral model in a simulation results in significant degradation

of simulation performance. Moreover, integration of the actual design model or vendor supplied behavioral model in the local simulation limits observability and controllability due to constraints stemming from the protection of proprietary data. A practical alternative to this problem is to develop an accurate custom behavioral model that offers sufficient parameters which can be programmed to represent framers from different vendors.

The present invention describes the architecture and implementation of a behavioral VHDL model of an ATM/SONET framer. The model is comprised of two independently configurable components, a Receiver and a Transmitter, and offers flexibility to allow testing with multiple vendors' of framers by changing programmable parameters of the model.

The present invention functions in the following manner. The basic architecture of the ATM/SONET FRAMER is shown in Fig. 1.

The invention offers the advantages of programmability, rich features set, and two independently configurable models, one each for transmit and receive

side. The programmability of the models extends beyond what is necessary to capture the functionality of commercial vendor devices.The programmable features include:

- SONET line rates (OC-Nc: N=1..48; OC-1=51.48 Mbps)
- Percentage of data bytes vs. overhead bytes per row
- Delays associated with clock domain synchronization
- FIFO depth and threshold (in terms of number of cells)
- Byte or word count threshold within a cell associated with FIFO status update
- UTOPIA Level-2/3
- Built-in performance checking

Framer Transmit Model

Features

- Insert ATM cells into a transmitted OC-Nc frame
- Insert idle cells for rate adaptation
- Provide interface setup and hold time checks
- Provide performance check

- Generate error messages if Utopia FIFO overrun or underrun during performance check
- Programmable Tx FIFO depth and threshold
- Latency associated with clock domain synchronization
- Programmable SONET rate

Description

The basic architecture of the ATM/SONET FRAMER is shown in Figure 1. The component represented as seen in the Fig. 1 are the network connections at location 100, the UUT (ATM Data Processor) at location 101, the Framer at 102, the ATM Clock Domain at location 103, the SONET Clock Domain at location 104.

Fig. 1, shows the implementation of transmit model, located at 105, which is implemented as a set of sixteen, per-port UTOPIA Tx FIFOs whose depth is settable by a generic parameter on the model, and a set of sixteen "virtual" network queues of infinite depth.

A UTOPIA Tx Level-2/3 physical bus interface process implements the utopia slave protocol and supports cell-level handshake and data transfer. Each cell

received from the UTOPIA Master Tx, location at 106, interface on the ATM UUT is written into the appropriate per-port UTOPIA Tx FIFO in the framer. The cell is then read out of the UTOPIA Tx FIFO (into the corresponding "virtual" network queue) based on a SONET framer process which follows the SONET overhead and SONET payload envelope (SPE) structure as shown in Fig. 2. There is one framer process per UTOPIA port. Each framer process can be configured independent of the others. Since multiple framers in a real system will power-up at random times, each framer process uses a built-in random delay between zero ns and one row time before starting to generate the virtual OC-Nc frames.

These framer processes constitute the core of the transmit model. Each process is synchronous to the SONET byte clock(which is programmable via the line rate parameter), and maintains a count of the cells received into the corresponding UTOPIA Tx FIFO. The process mimics the SONET frame structure by maintaining a running count of the overhead bytes received for a row, the count of data bytes received for the cell, and the count of rows

within the fixed 125 micro-second frame length. When the running count of data bytes received for a cell equals 53 (the number of bytes in an ATM cell) the cell count in the UTOPIA Tx FIFO is decremented.

Since, the SONET frames length is independent of the SONET data rate and fixed at 125 micro-seconds , the parameters such as the number of bytes in a row and the number of bytes in SONET payload envelope can be modified by programming different values of the line rate, and/or the percentage of data bytes in a row. These values may be set from a test case via a procedure call to the framer model.

Many vendors' framer provide programmability in FIFO status update during Write and Read. A cell is generally not transmitted until the complete cell has been written into the Tx FIFO. The programmability feature allows the cell count to be incremented before the entire cell is physically transferred. This is specified in terms of number of words transferred across the UTOPIA interface. The model supports this programmability via a generic. Similarly, the cell count is decremented when a complete cell from Tx FIFO is inserted into the SONET frame. The

cell count can be decremented at a programmable byte count into the ATM cell structure. This feature is also supported via a different generic. Two additional generics have been included in the model to mimic the synchronization delay between ATM and SONET clock domains. These two generics represent the latency associated with propagation and registration of FIFO status (cell count) update across the ATM/SONET domain boundary in each direction.

This model can be programmed to handle UTOPIA Level-2/3 via a generic. Each port can be programmed to emulate a particular SONET line rate (0 to 2488.32 Mbps).

Framer Receive Model

Features

- Extract ATM cells from the received OC-Nc frame format.
- Strip idle cells
- Purge enqueued cells
- Provide interface setup and hold time checks
- Provide performance check on the line side

- Generate error messages if UTOPIA Rx FIFO overrun or underrun during performance check
- Programmable Rx FIFO depth and threshold
- Latency associated with clock domain synchronization
- Programmable SONET rate

Description

As shown in Fig. 1, the SONET receive model is implemented as two logical sets of sixteen, per-port FIFOs. The sixteen network FIFOs are infinitely deep. The depth of UTOPIA Rx FIFOs defaults to a value of four cells, and can be modified via a procedure call.

ATM cells are enqueued to the receive model via a procedure call from a test case, and are placed in the appropriate per-port network FIFO. The cell is then read out of the network FIFO and written into the corresponding UTOPIA Rx FIFO based on a framer process which mimics the SONET overhead and payload envelope structure. There is one framer process for each port, and each framer process can be configured independently of the others. A UTOPIA Rx Level-2/3 physical bus

interface process implements the slave protocol and supports cell-level handshake and forwards the cells from UTOPIA Rx FIFO to the UUT.

The framer processes are synchronous to the SONET byte clock, which is programmable via the line rate, and maintains a count of data bytes (versus overhead bytes) in a cell, and a count which represents the number of rows in a 125 micro-seconds SONET frame. On the simulation start-up, these processes delay a random amount of time (between 0 ns and one row time) before starting to emulate extraction of ATM cells from the SONET frame structure in order to mimic the random start of different framers.

A cell is received into the UTOPIA Rx FIFO and cell count incremented when the count of data bytes in a cell extracted from the SONET frame equals a generic parameter. The default value of this parameter is set to 53. Similarly, when the count of words in a cell which have been transferred across the UTOPIA Rx bus equals another generic, the count of cells in the UTOPIA Rx FIFO is decremented. The synchronization delay between ATM and

SONET clock domains, observed in real framer implementations, is modeled by two additional generics. These two generics represent the latency associated with propagation and registration of FIFO status (cell count) update across the ATM/SONET domain boundary in each direction.

This model can be programmed to handle UTOPIA Level-2/3 via a generic. The model supports randomization of ATM cell payload. Each port can be programmed to emulate a particular SONET line rate (0 to 2488.32 Mbps).

While the invention has described with respect to a specific embodiment, it will be obvious to those skilled in this art that changes in ~~both form~~ and/or detail may be made without a departure from the scope and/or spirit of the invention.

We claim: